# EDOSK2674

USER MANUAL

FOR H8/2674R
MICROCOMPUTER

## Preface

## Cautions

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## Document Information

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# Table of Contents

# 1. INTRODUCTION

The EDOSK2674 is an Evaluation Development Operating System Kit designed around the Hitachi H8/2674R microcomputer (MCU).

The EDOSK2674 operates from a single 5V supply.

Only two modes of operation: Boot mode and Normal mode.

33MHz bus clock speed.

The EDOSK2674 card provides the following interfaces:

- One serial communication interface up to 115200kbs with no errors.
- A standard RJ45 Ethernet interface provides connection to a Local Area Network (includes Link and Activity indicators).
- A 140-way high-density connector for interface to a bus expansion card.
- Position for a 50 way Auxiliary I/O header to allow connection to all unused MCU I/O pins and power.

The EDOSK2674 card is provided with the following memory types and densities:

- 512KBytes (8-bit x 512) Boot Flash memory
- 4MBytes (16-bit x 2M) Main Flash memory
- 8MBytes (16-bit x 4bank x 1M) SDRAM memory

A Real-time clock (RTC) is fitted to the EDOSK2674 to provide current date and time information to the MCU.

## 1.1. EDOSK2674 GENERAL BOARD LAYOUT

The general board layout shows the position of all major parts of the board.

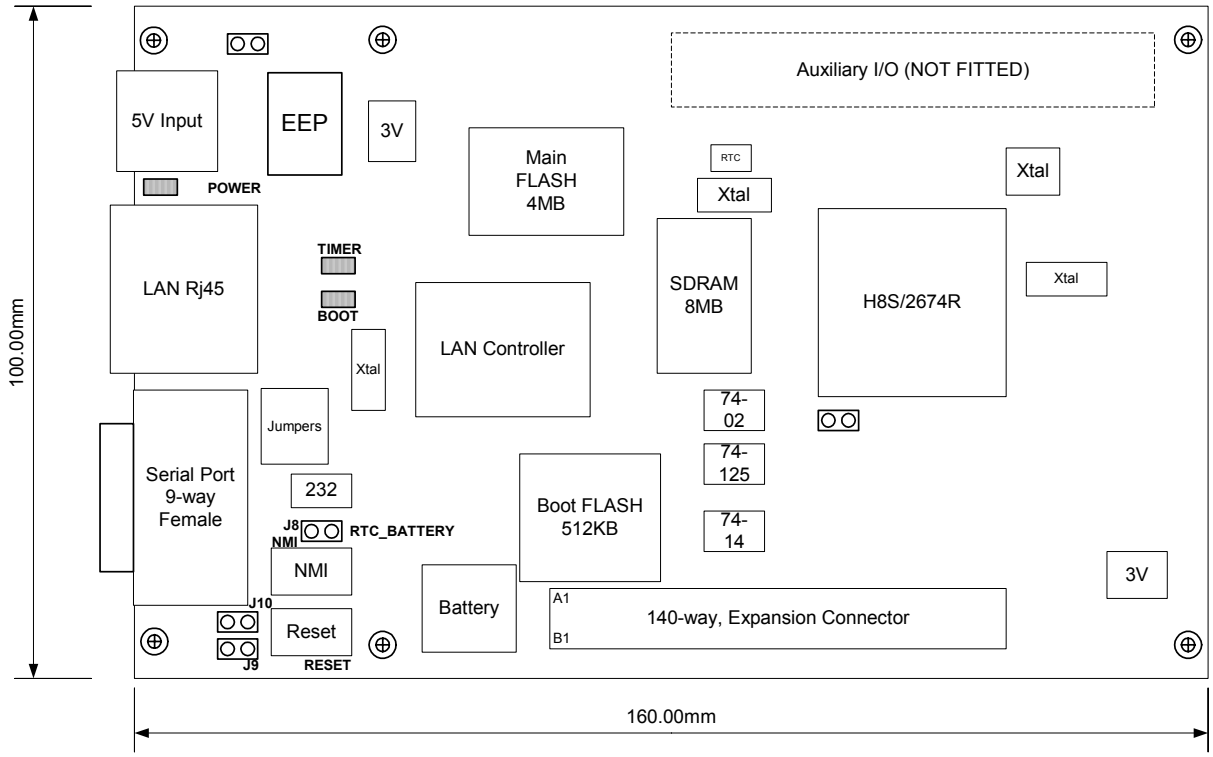



**Figure 1-1: EDOSK General Board Layout**

## 1.2. EDOSK2674 ACTUAL BOARD LAYOUT

The actual board layout shows the real position of all components, the reference numbers and silk screen labelling.

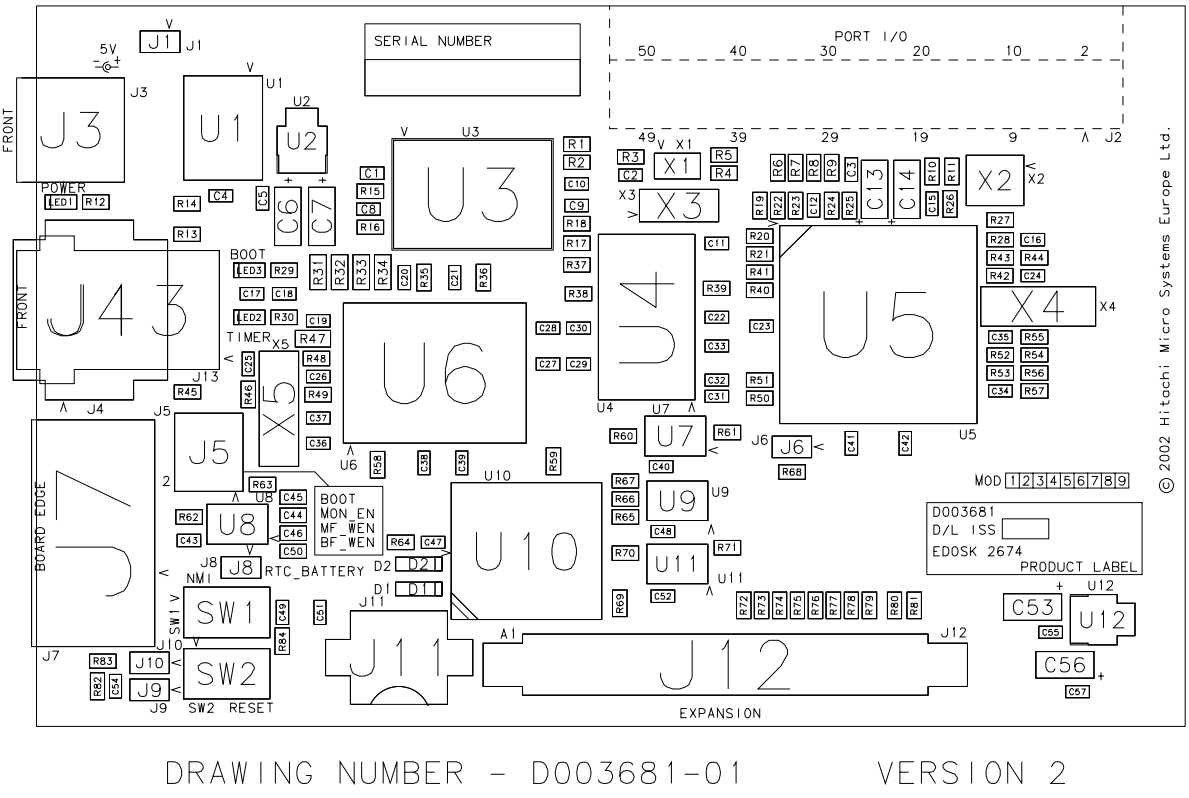



**Figure 1-2: EDOSK Actual Board Layout**

# 2. EDOSK2674 BLOCK DIAGRAM

The EDOSK2674 is designed around a H8/2674R MCU and includes FLASH memory, SDRAM, real-time clock, an interface to a local expansion card, an interface for IO connections, a serial port and a LAN port.

The figure below shows the block diagram of the EDOSK2674 board.

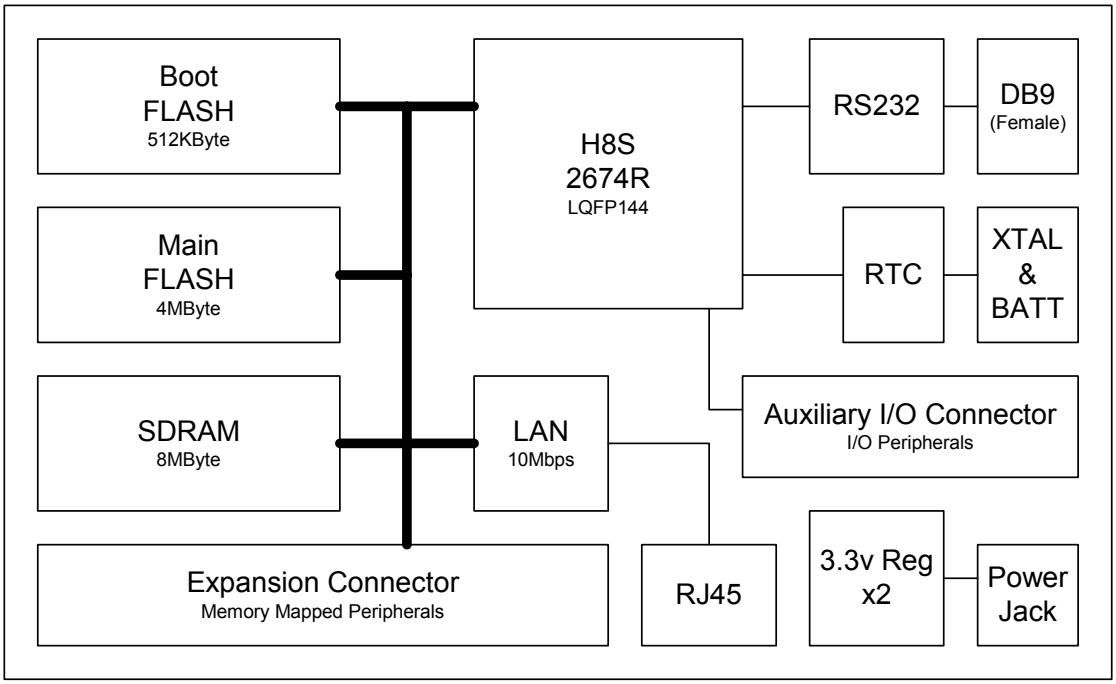



FIGURE 2-1: EDOSK BLOCK DIAGRAM

## 2.1. POWER SUPPLY

The EDOSK hardware requires a power supply of +5V. Since total power consumption can vary widely due to external connections, port states, and memory configuration, use a power supply capable of providing at least 500mA at +5V DC ± 5%.

The design is specified for evaluation of the MCU and so does not include circuitry for supply filtering/noise reduction, under voltage protection, over current protection or reversed polarity protection. Caution should be used when selecting and using a power supply.

The power connector on the EDOSK is a 2.5mm Barrel connector. The center pin is the positive connection.

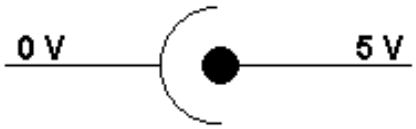



FIGURE 2-2: POWER SUPPLY CONNECTION

**Caution: Existing customers using E6000 products note that the polarity of this board is opposite to that for the E6000. Use of the E6000 power supply with this board will damage both board and power supply.**

## 2.2. OPERATING MODES

The H8/2674R has only two modes of operation set by jumper configuration:

Mode 1: (MD2=0, MD1=0, MD0=1) Advanced, External Data Bus initial Width is 16 bits. – EDOSK NORMAL mode.

Mode 2: (MD2=0, MD1=1, MD0=0) Advanced, External Data Bus initial Width is 8 bits. – EDOSK BOOT mode.

The H8/2674R has no internal Flash memory. On power-up the EDOSK mode (Boot or Normal) selects the Flash memory from which the H8/2674R first accesses.

## 2.3. H8/2674R MICROCOMPUTER

The MCU is an H8/2674R derivative of the H8/2600 series microprocessor with an internal 16-bit architecture, sixteen 16-bit general registers and 69 basic instructions.

The MCU contains a number of on-chip facilities, including:

- 33MHz maximum operating frequency
- Voltage: 3.3V
- 24 bit external address bus, 16 bit external data bus
- 33MHz max external bus frequency
- 7 areas of external address space, each 2MBytes
- Supports direct SDRAM interface
- Various peripheral functions:
    - DMA controller (DMAC)
    - EXDMA controller (EXDMAC)
    - Data transfer controller (DTC)
    - 16-bit timer-pulse unit (TPU)
    - Programmable pulse generator (PPG)
    - 8-bit timer (TMR)
    - Watchdog timer (WDT)
    - Asynchronous serial communication interface (SCI)
    - 10-bit A/D converter
    - 8-bit D/A converter
    - Clock pulse generator
- On-chip memory:
    - 32Kbytes RAM
- General I/O ports:
    - I/O pins: 103
    - Input-only pins: 12

## 2.4. BOOT FLASH MEMORY

The BOOT Flash memory is a 512K x 8bit PLCC device (AMD 29LV040B) and is fitted to a socket on the EDOSK2674.

The MCU interfaces with the BOOT Flash on reset in area 0 only when the EDOSK is set to Boot mode.

The same BOOT Flash is also accessible in area 7 when the EDOSK is set to either Boot or Normal mode.

In Normal mode the BOOT Flash is designed to reside in area 7 only.

The BOOT Flash may be removed from its socket to be programmed by a dedicated programmer or alternately it may be programmed in system when the Boot write enable jumper is fitted.

Details of BSC register settings for the AMD Flash boot memory can be found in section 7.2.

Boot Flash access:

- Bus Width: 8 bit.
- Access States: 3
- Wait States: 3
- Cycle Burst: 6 (area 0 only)

Extended CS period: $T_h$ and $T_t$ (area 7 only)

## 2.5. MAIN FLASH MEMORY

The MAIN Flash memory is a 4MByte device (INTEL 28F320J3A) and is word accessed.

The MCU interfaces with the MAIN Flash on reset in area 0 only when the EDOSK is set to Normal mode.

In Normal mode the MAIN Flash is designed to reside in area 0 and area 1.

In Boot mode the MAIN Flash is designed to reside in area 1 only and is paged by driving port pin 33.

The Main Flash may be programmed in system when write enable jumper is fitted.

Details of BSC register settings for the Intel Flash memory can be found in section 7.2.

Main Flash access:

Bus Width: 16 bit.

Access States: 3

Wait States: 2

Cycle burst: 6

## 2.6. RAM

The H8/2674R has 32KB of RAM available on-chip. This RAM can be enabled or disabled by means of the RAME bit in the system control register (SYSCR). Initially this RAM is enabled.

## 2.7. SDRAM

The H8/2674R, external address space areas 2 to 5, has been designated as continuous Synchronous DRAM space. An 8MB external SDRAM interfaces directly to the MCU.

The SDRAM used is a MICRON MT48LC4M16A2:

Row addressing: 4K (A0-A11)

Bank addressing: 4 (BA0, BA1)

Column addressing: 512 (A0-A8)

MCU port pin 34 is used to drive the SDRAM CS pin.

Details of BSC and DRAM register settings for the SDRAM can be found in section 7.2.

SDRAM access:

Bus Width: 16 bit.

## 2.8. LAN CONTROLLER

The LAN controller IC is a SMSC LAN91C96 device. The base address of this device defaults to 300h, however the EDOSK re-maps this to F80000h.

The MAC address is contained within a removable EEPROM connected to the Controller. This is programmed during production testing and should not be altered.

Details of BSC register settings for the LAN controller can be found in section 7.2.

LAN Controller access:

Bus Width: 8 bit.

Access States: 3

Wait States: 3

Extended CS period: $T_h$ and $T_t$

## 2.9. REAL TIME CLOCK

The EDOSK is supplied with a Real Time Clock (RTC) and battery backup (when fitted) for current date and time information.

A cell retainer (J11) is used to hold a cell battery to keep time data correct when system supply is removed.

The RTC is a Dallas/Maxim DS1672U device that interfaces to the H8/2674R via an I2C bus.

- SCL – Serial Clock (MCU port pin 31)
- SDA – Serial Data (MCU port pin 32)

A coin-cell battery between 1.3V and 3.6V of 12mm diameter and 3.175mm maximum height may be inserted into the EDOSK to allow timekeeping even when power to the board is removed.

Battery Reference: BR1216, CR1216, BR1220, CL1220, CR1220 and BR1225

## 2.10. SWITCHES

The EDOSK provides two buttons for influencing the operation of the board. The purpose of each button is clearly marked next to it. Refer to the board layout for positions (Section 1).

- **Reset Switch**

  This button provides the MCU with a timed reset pulse of at least 250mS.

- **NMI Switch**

  The NMI button on this EDOSK provides the MCU with a positive pulse to generate a non-maskable interrupt.

## 2.11. INDICATORS

Three red LEDs are fitted to the PCB. The function of each red LED is clearly marked on the silk screen of the PCB. Please refer to the board layout diagram for position information (Section 1).

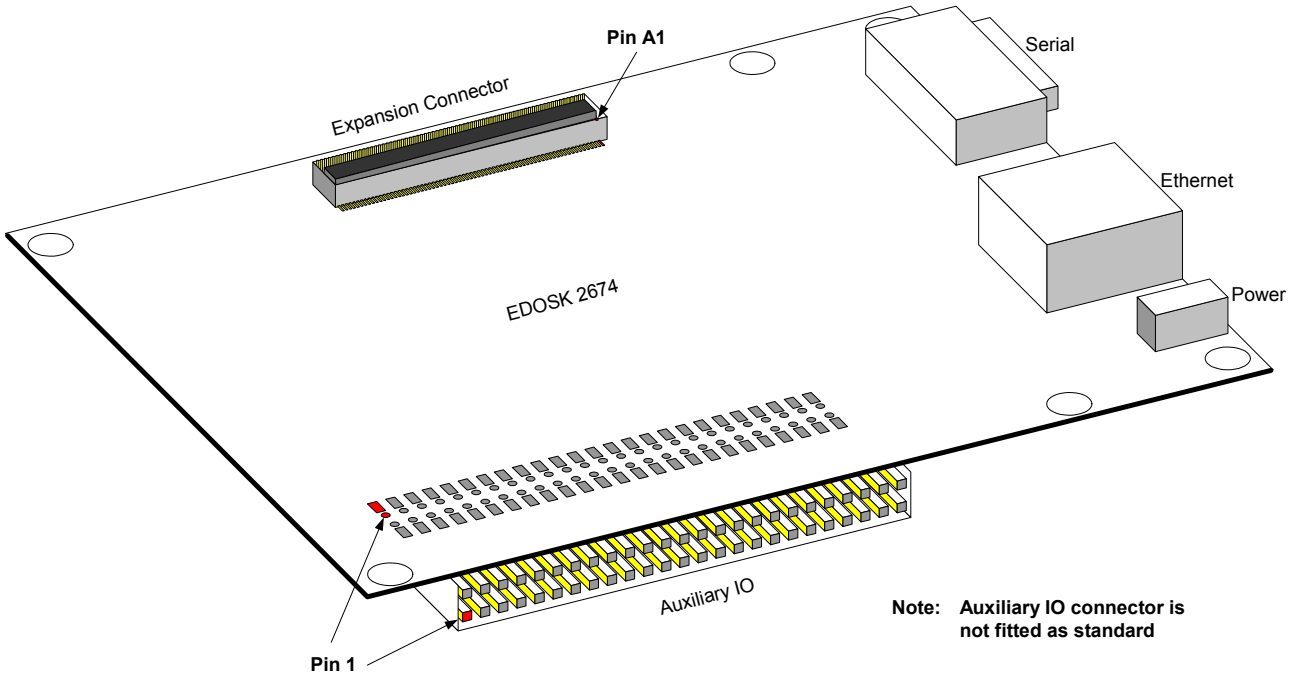
POWER: When the board is connected to a power source this led will illuminate.

BOOT: When the EDOSK has been placed into Boot mode this LED will illuminate.

TIMER: Dedicated for user control and is driven by the MCU Watchdog Timer Overflow pin.

# 3. EXTERNAL INTERFACES

Connector locations and pin orientation for Expansion and Auxiliary IO (right-angled 50-way IDC) is shown below:




## 3.1. SERIAL INTERFACE

The Serial Communication Interface (SCI-3) on the MCU directly supports three-wire serial interfaces.

The EDOSK provides the MCU with an external clock source at 1.8432MHz. This provides a fixed baud rate of 11520kbps for the serial port with zero errors (irrespective of the operating crystal frequency).

A hyper terminal link between the EDOSK and a PC will enable the user interface.

- Link to a Hyper Terminal
- Connect at baud rate 115200, 8 bits, no parity, 1 stop bit

The EDOSK RS232 interface conforms to Data Communication Equipment (DCE) format allowing the use of 1-1 cables when connected to Data Terminal Equipment (DTE) such as an IBM PC. Handshaking is not supported as standard on the MCU so for normal use a minimal three-wire cable can be used. The minimum connections are not shaded in the following table.

| EDOSK DB9 Connector Pin | Signal | Host DB9 Connector Pin |
|---|---|---|
| 1 | No Connection | 1 |
| 2 | EDOSK Tx Host Rx | 2 |
| 3 | EDOSK Rx Host Tx | 3 |
| 4 | No Connection | 4 |
| 5 | Ground | 5 |
| 6 | No Connection | 6 |
| 7 | No Connection | 7 |
| 8 | No Connection | 8 |
| 9 | No Connection | 9 |

TABLE 3-1: RS232 INTERFACE CONNECTIONS

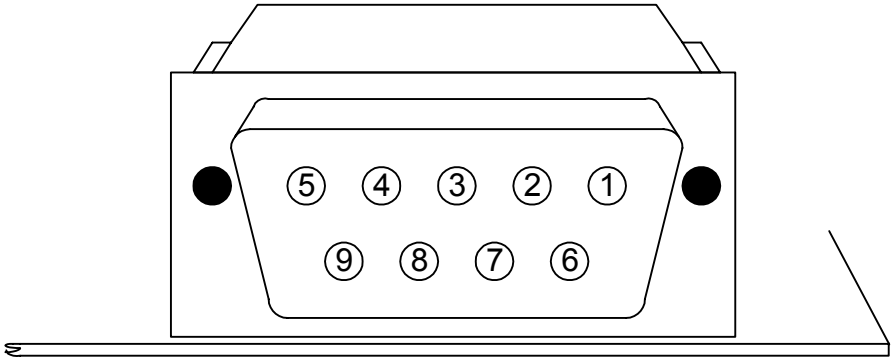



**Figure 3-1: EDOSK Serial Port Pin Numbering**

## 3.2. LAN INTERFACE

A 10MHz LAN connection is provided through a standard RJ45 interface.

Two LEDs are integrated into the Ethernet connector and give the following indication:

Green: Link Indicator. Reflects the integrity status.

Yellow: Activity Indicator. Activated by Transmit or Receive activity.

| Pin | Name | Direction | Description |
|---|---|---|---|
| RJ1 | TxD+ | Output from the EDOSK | Transmit Data Positive |
| RJ 2 | TxD- | Output from the EDOSK | Transmit Data Negative |
| RJ 3 | RxD+ | Input from the LAN | Receive Data Positive |
| RJ 4 | N/C | Not Connected | |
| RJ 5 | N/C | Not Connected | |
| RJ 6 | RxD- | Input from the LAN | Receive Data Negative |
| RJ 7 | N/C | Not Connected | |
| RJ 8 | N/C | Not Connected | |

**TABLE 3-2: LAN INTERFACE CONNECTIONS**

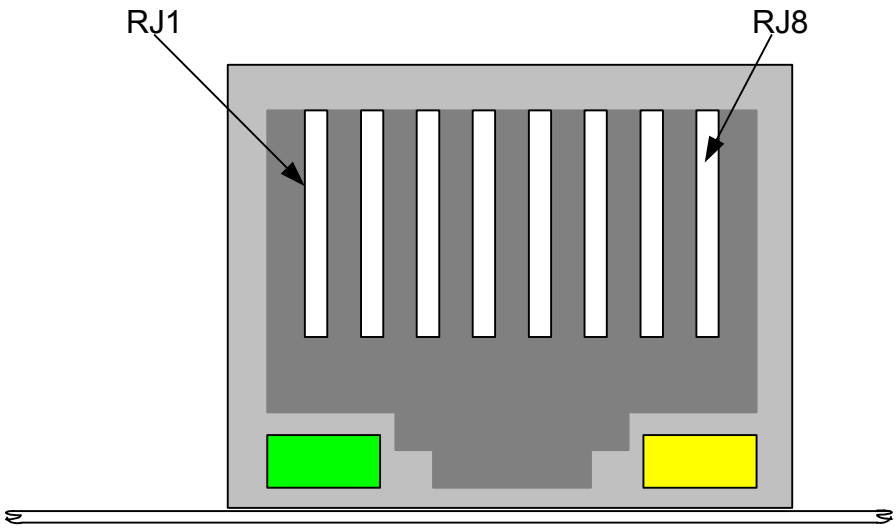



**Figure 3-2: EDOSK LAN Port Pin Numbering**

## 3.3. EXPANSION CONNECTOR

The EDOSK expansion bus connector is a 140-way JAE KX14-140K5D and has the following pin connections:

| Col: A | Assignment | Type | I/O | H8S2674R | Col: B | Assignment | Type | I/O | H8S2674R |
|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | - | - | GND | 1 | GND | - | - | GND |
| 2 | CKIO | O | OUT | Sys. Clk | 2 | GND | - | - | GND |
| 3 | GND | - | - | GND | 3 | GND | - | - | GND |
| 4 | D0 | T | I/O | D0 | 4 | D1 | T | I/O | D1 |
| 5 | D2 | T | I/O | D2 | 5 | D3 | T | I/O | D3 |
| 6 | D4 | T | I/O | D4 | 6 | D5 | T | I/O | D5 |
| 7 | D6 | T | I/O | D6 | 7 | D7 | T | I/O | D7 |
| 8 | GND | - | - | GND | 8 | GND | - | - | GND |
| 9 | D8 | T | I/O | D8 | 9 | D9 | T | I/O | D9 |
| 10 | D10 | T | I/O | D10 | 10 | D11 | T | I/O | D11 |
| 11 | D12 | T | I/O | D12 | 11 | D13 | T | I/O | D13 |
| 12 | D14 | T | I/O | D14 | 12 | D15 | T | I/O | D15 |
| 13 | GND | - | - | GND | 13 | GND | - | - | GND |
| 14 | D16 | T | I/O | No Connect | 14 | D17 | T | I/O | No Connect |
| 15 | D18 | T | I/O | No Connect | 15 | D19 | T | I/O | No Connect |
| 16 | D20 | T | I/O | No Connect | 16 | D21 | T | I/O | No Connect |
| 17 | D22 | T | I/O | No Connect | 17 | D23 | T | I/O | No Connect |
| 18 | GND | - | - | GND | 18 | GND | - | - | GND |
| 19 | D24 | T | I/O | No Connect | 19 | D25 | T | I/O | No Connect |
| 20 | D26 | T | I/O | No Connect | 20 | D27 | T | I/O | No Connect |
| 21 | D28 | T | I/O | No Connect | 21 | D29 | T | I/O | No Connect |
| 22 | D30 | T | I/O | No Connect | 22 | D31 | T | I/O | No Connect |
| 23 | 3.3V | - | - | 3.3V | 23 | 3.3V | - | - | 3.3V |
| 24 | 3.3V | - | - | 3.3V | 24 | 3.3V | - | - | 3.3V |
| 25 | NC0 | Option | Option | No Connect | 25 | 3.3V | - | - | 3.3V |
| 26 | A0 | O | OUT | A0 | 26 | A1 | O | OUT | A1 |
| 27 | A2 | O | OUT | A2 | 27 | A3 | O | OUT | A3 |
| 28 | A4 | O | OUT | A4 | 28 | A5 | O | OUT | A5 |
| 29 | A6 | O | OUT | A6 | 29 | A7 | O | OUT | A7 |
| 30 | GND | - | - | GND | 30 | GND | - | - | GND |
| 31 | A8 | O | OUT | A8 | 31 | A9 | O | OUT | A9 |
| 32 | A10 | O | OUT | A10 | 32 | A11 | O | OUT | A11 |
| 33 | A12 | O | OUT | A12 | 33 | A13 | O | OUT | A13 |
| 34 | A14 | O | OUT | A14 | 34 | A15 | O | OUT | A15 |
| 35 | GND | - | - | GND | 35 | GND | - | - | GND |
| 36 | A16 | O | OUT | A16 | 36 | A17 | O | OUT | A17 |
| 37 | A18 | O | OUT | A18 | 37 | A19 | O | OUT | A19 |
| 38 | A20 | O | OUT | A20 | 38 | A21 | O | OUT | A21 |
| 39 | A22 | O | OUT | A22 | 39 | A23 | O | OUT | A23 |
| 40 | A24 | - | - | No Connect | 40 | A25 | O | OUT | No Connect |
| 41 | GND | - | - | GND | 41 | GND | - | - | GND |
| 42 | /DACK0 | O | OUT | /DACK0 | 42 | /DACK1 | O | OUT | /DACK1 |
| 43 | /DREQ0 | I, P-UP | IN | /DREQ0 | 43 | /DREQ1 | I, P-UP | IN | /DREQ1 |
| 44 | GND | - | - | GND | 44 | GND | - | - | GND |
| 45 | /CS0 | O, P-UP | OUT | /CS0 | 45 | /CS1 | O, P-UP | OUT | /CS1 |
| 46 | /CS2 | O | OUT | No Connect | 46 | /CS3 | O | OUT | No Connect |
| 47 | /CS4 | O | OUT | No Connect | 47 | /CS5 | O | OUT | No Connect |
| 48 | /CS6 | O, P-UP | OUT | /CS6 | 48 | R/W | O | OUT | No Connect |
| 49 | GND | - | - | GND | 49 | GND | - | - | GND |
| 50 | /RD | O | OUT | /RD | 50 | /BS | O | OUT | /AS |

| Col: A | Assignment | Type | I/O | H8S2674R | Col: B | Assignment | Type | I/O | H8S2674R |
|---|---|---|---|---|---|---|---|---|---|
| **51** | GND | - | - | GND | **51** | GND | - | - | GND |
| **52** | /WE0 | O | OUT | /LWR | **52** | /WE1 | O | OUT | /HWR |
| **53** | /WE2 | O | OUT | No Connect | **53** | /WE3 | O | OUT | No Connect |
| **54** | GND | - | - | GND | **54** | GND | - | - | GND |
| **55** | /WAIT0 | I, P-UP | IN | /EXP_WAIT | **55** | /WAIT1 | I, P-UP | IN | No Connect |
| **56** | /WAIT2 | I, P-UP | IN | No Connect | **56** | /WAIT3 | I, P-UP | IN | No Connect |
| **57** | GND | - | - | GND | **57** | GND | - | - | GND |
| **58** | /IRQ1 | I, P-UP | IN | /IRQ1 | **58** | /IRQ2 | I, P-UP | IN | /IRQ2 |
| **59** | /IRQ3 | I, P-UP | IN | /IRQ3 | **59** | /IRQ4 | I, P-UP | IN | /IRQ4 |
| **60** | /IRQ5 | I, P-UP | IN | /IRQ5 | **60** | /IRQ6 | I, P-UP | IN | No Connect |
| **61** | /IRQ7 | I, P-UP | IN | No Connect | **61** | /IRQ8 | I, P-UP | IN | No Connect |
| **62** | +5V | - | - | +5V | **62** | +5V | - | - | +5V |
| **63** | +5V | - | - | +5V | **63** | +5V | - | - | +5V |
| **64** | NC1 | Option | Option | No Connect | **64** | +5V | - | - | +5V |
| **65** | /RES | O | OUT | /RESET | **65** | +5V | - | - | +5V |
| **66** | A+5V | - | - | +5V | **66** | +5V | - | - | +5V |
| **67** | A+5V | - | - | +5V | **67** | NC2 | Option | Option | No Connect |
| **68** | NC3 | Option | Option | No Connect | **68** | NC4 | Option | Option | No Connect |
| **69** | NC5 | Option | Option | No Connect | **69** | NC6 | Option | Option | No Connect |
| **70** | NC7 | Option | Option | No Connect | **70** | NC8 | Option | Option | No Connect |

**TABLE 3-3: EXPANSION BUS CONNECTIONS**

O = Not buffered output. I = Not buffered input. P-UP = Pull up resistor.

Expansion cards to be fitted to the EDOSK should use JAE connector KX15-140K2D and should only have discrete components fitted to the under side with a maximum height of 2mm.

## 3.4. AUXILIARY I/O HEADER

Position for a 50 way Auxiliary I/O header is provided on the EDOSK to allow connection to all unused MCU I/O pins and power.

This part has not been fitted as standard because it has been recognised that the user will wish to select the connector type.

Through holes and surface mount pads allow for a number of connector options:

- SM pins fitted on top or under the PCB – Samtec TSM-125-0X-X-DV
- SM sockets on top or under the PCB – Samtec SSM-125-X-DV
- Any through hole 50-way connector at 0.1" pitch.

| I/O Conn | MCU Pin | Symbol | I/O Conn | MCU Pin | Symbol |
|---|---|---|---|---|---|
| 1 | N/A | No Connect | 2 | N/A | 5V |
| 3 | 131 | AVSS | 4 | N/A | GND |
| 5 | 84 | P65 | 6 | 83 | P64 |
| 7 | 82 | P63 | 8 | 81 | P62 |
| 9 | 110 | P53 | 10 | 113 | PG4 |
| 11 | 114 | PG5 | 12 | 115 | PG6 |
| 13 | 121 | VREF | 14 | 122 | AVCC |
| 15 | 117 | P40 | 16 | 118 | P41 |
| 17 | 119 | P42 | 18 | 120 | P43 |
| 19 | 123 | P44 | 20 | 124 | P45 |
| 21 | 125 | P46 | 22 | 126 | P47 |
| 23 | 127 | P54 | 24 | 93 | STBYn |
| 25 | 129 | P56 | 26 | 128 | P55 |
| 27 | 61 | P61 | 28 | 130 | P57 |
| 29 | 59 | P27 | 30 | 60 | P60 |
| 31 | 57 | P25 | 32 | 58 | P26 |
| 33 | 55 | P23 | 34 | 56 | P24 |
| 35 | 53 | P21 | 36 | 54 | P22 |
| 37 | 51 | P17 | 38 | 52 | P20 |
| 39 | 49 | P15 | 40 | 50 | P16 |
| 41 | 46 | P13 | 42 | 48 | P14 |

| I/O Conn | MCU Pin | Symbol | I/O Conn | MCU Pin | Symbol |
|---|---|---|---|---|---|
| 43 | 44 | P11 | 44 | 45 | P12 |
| 45 | 40 | P73 | 46 | 43 | P10 |
| 47 | 36 | P72 | 48 | N/A | GND |
| 49 | N/A | No Connect | 50 | N/A | 3V3 |

**TABLE 3-4: AUXILIARY I/O CONNECTIONS**

# 4. BOARD OPTIONS

## 4.1. JUMPER LINKS

The EDOSK has a two-row 8 pin header for selecting operation modes.

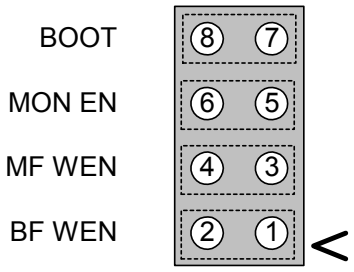



FIGURE 4-1: JUMPER CONFIGURATION

As default, jumpers for BOOT and MF WEN are fited.

**BOOT: Boot/Normal Mode.**

Fitted to link pins 8-7 – Boot Mode: MCU initialises in 8-bit mode and boots from the 512KB Boot FLASH.

Not fitted – Normal Mode: Micon initialises in 16-bit mode and boots from the 4MB Main FLASH.

**MON EN: Monitor Enable.**

Fitted to link pins 6-5 – Enables the Hitachi monitor (when included in user code).

Not fitted – Program code runs with no monitor.

**MF WEN: Main FLASH Write Enable.**

Fitted to link pins 4-3 – Allows the Main FLASH to be written to by the MCU.

Not fitted – Main FLASH is write protected.

**BF WEN: Boot FLASH Write Enable.**

Fitted to link pins 2-1 – Allows the Boot FLASH to be written to by the MCU.

Not fitted – Boot FLASH is write protected.

## 4.2. RTC BACKUP SUPPLY

Without a backup supply to the RTC, time and date information is lost when the board is powered down.

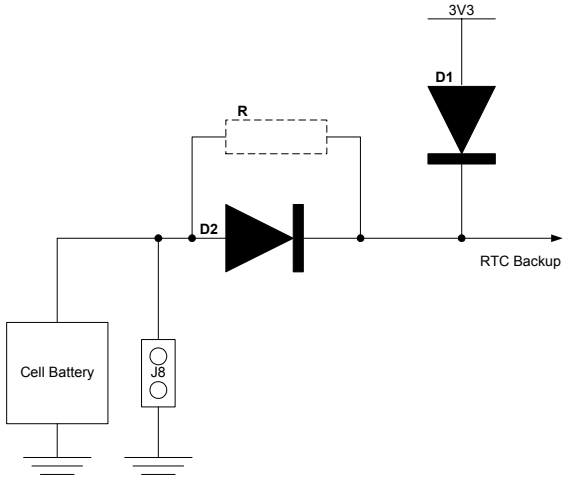
Two options are available on the EDOSK:

1. A cell battery may be fitted.
2. An auxiliary supply of 1.3V to 3.6V may be provided to J8 – a 2-pin through hole header (not fitted).

Each of these options may or may not be rechargeable.

If however neither option is used or the backup supply falls below 1.3V then the EDOSK board will cease to function when powered up unless a supply from Vcc is provided. By default design this supply from Vcc is provided.

The Following diagram shows the circuit used for the RTC backup supply:




D1 provides the Vcc supply and prevents the cell battery (or auxiliary supply) from powering all of the board when powered down.

D2 provides protection for the cell battery (or auxiliary supply) against accidental charging.

R (when fitted) allows charge current to be selected or charging by the RTC device.

The following options are available:

| Backup power option | Component configuration | Comments |
|---|---|---|
| No cell battery, No auxiliary supply, None rechargeable cell battery, None rechargeable auxiliary supply | D1 and D2 fitted.<br>R not fitted. | Default configuration.<br>No method of recharging cell or auxiliary supply. |
| Rechargeable cell battery, Rechargeable auxiliary supply | D1 and D2 fitted.<br>R not fitted. | Default configuration.<br>No method of recharging cell or auxiliary supply. |
| | D1 fitted.<br>D2 optional.<br>$R=3.3/I_{charge}$ | Backup supply is charged through D1.<br>RTC trickle charge is not used. |
| | D1 not Fitted.<br>D2 optional.<br>R=0 ohms. | Backup supply is charged through<br>RTC trickle charge network.<br>EDOSK will not operate if backup supply fails. |

## 4.3. REMOTE SWITCH

Both Reset and NMI switches may be activated remotely.

By attaching 2-pin headers to J10 and J9, normally-open switches can be attached via flying leads.

J10 – NMI

J9 – RESET

The NMI switch signal is de-bounced on the EDOSK board with a time constant $T_{RC}$=0.47 seconds.

The RESET switch signal is de-bounced on the EDOSK board with time constants $T_{RC(off)}$=0.03 seconds and $T_{RC(on)}$=0.22 seconds.

## 4.4. CRYSTAL CHOICE

The MCU crystal frequency has been chosen to support the fastest operation. The value of the crystal is 33.0000MHz.

The user may replace the HC49/U surface mounted AT cut crystal with another of similar type within the operating frequency of the MCU device. Please refer to the hardware manual for the MCU for the valid operating range.

Another crystal is provided at 16 x 115200 (1.8432MHz). This crystal output is fed directly into the SCK2 pin of the MCU allowing, with correct register settings, a fixed serial baud rate of 115200bps with zero errors.

The user may wish to ignore the serial clock oscillator input and use the system clock for baud rate generation – register settings will need to be amended as per the following example.

Example:

The following table shows the baud rates and Baud Rate Register (BRR) setting required for each communication rate using the operating speed of **33.0000MHz** (default). Note that there are no zero error percentages.

| **Baud Rate Register Settings for Serial Communication Rates using 33.0000MHz system clock** | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **SMR Setting:** | **0** | | **1** | | **2** | | **3** | |
| **Comm. Baud** | **BRR setting** | **ERR (%)** | **BRR setting** | **ERR (%)** | **BRR setting** | **ERR (%)** | **BRR setting** | **ERR (%)** |
| **110** | Invalid | Invalid | Invalid | Invalid | Invalid | Invalid | 145 | 0.33 |
| **300** | Invalid | Invalid | Invalid | Invalid | 214 | 0.07 | 53 | 0.54 |
| **1200** | Invalid | Invalid | 214 | 0.07 | 53 | 0.54 | 12 | 3.29 |
| **2400** | Invalid | Invalid | 106 | 0.39 | 26 | 0.54 | 6 | 4.09 |
| **4800** | 214 | 0.07 | 53 | 0.54 | 12 | 3.29 | 2 | 11.90 |
| **9600** | 106 | 0.39 | 26 | 0.54 | 6 | 4.09 | 1 | 16.08 |
| **19200** | 53 | 0.54 | 12 | 3.29 | 2 | 11.90 | 0 | 16.08 |
| **38400** | 26 | 0.54 | 6 | 4.09 | 1 | 16.08 | Invalid | Invalid |
| **57600** | 17 | 0.54 | 3 | 11.90 | 0 | 11.90 | Invalid | Invalid |
| **115200** | 8 | 0.54 | 1 | 11.90 | 0 | 44.05 | Invalid | Invalid |

**TABLE 4-1 CRYSTAL FREQUENCIES FOR RS232 COMMUNICATION**

## 4.5. REMOVABLE COMPONENT INFORMATION.

Analogue and reference voltages to the MCU are, as default, isolated from the Auxiliary I/O connector by not fitted 0805 resistors. To make this connection the following resistors must be removed and re-soldered or replaced in the alternative positions detailed below:

| **H8/2674R pin** | **Remove** | **Fit** | **Resistor Value** |
|---|---|---|---|
| AVCC (pin 122) | R25 | R9 | 0Ω, 0805 |
| AVSS (pin 131) | R7 | R8 | 0Ω, 0805 |
| VREF (pin 121) | R11 | R10 | 0Ω, 0805 |

Care must be taken not to damage the tracking around these components. Only use soldering equipment designed for surface mount assembly and rework.

## 4.6. ADDITIONAL COMPONENT INFORMATION.

The addition of a 0Ω resistor fitted in position R37 will permanently deactivate the Main Flash. This is to be used when CS0n and/or CS1n are to be used by an Expansion Board.

## 5. START-UP INSTRUCTIONS

1. Connect the EDOSK to a PC or notebook computer equipped with a nine pin D connector using a direct 1-1 cable (supplied).

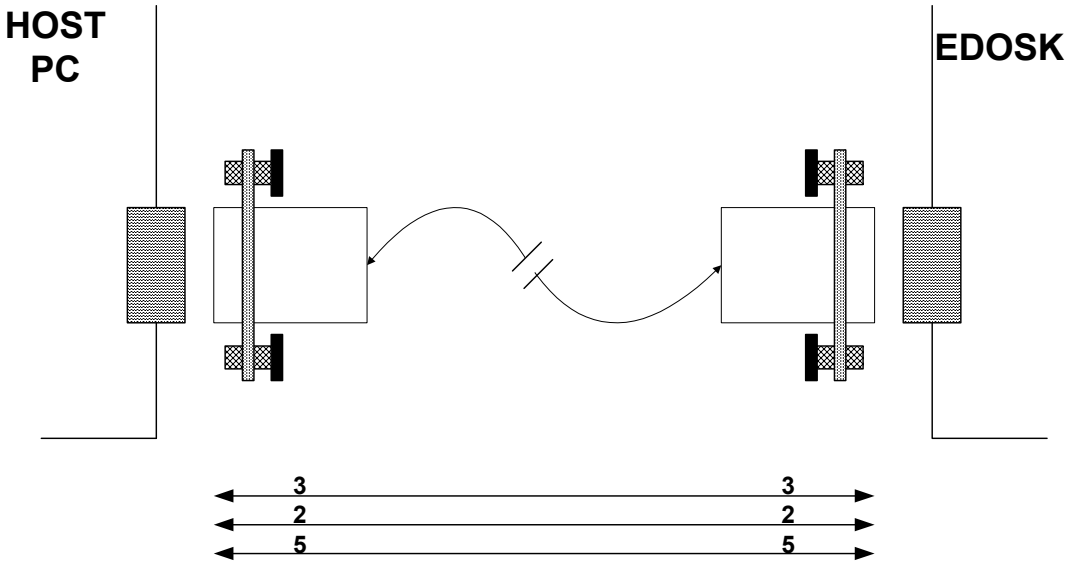



FIGURE 5-1: SERIAL CONNECTION TO PC/NOTEBOOK WITH DB-9 CONNECTOR (SUPPLIED)

2. Open a Hyper terminal set to a baud rate of 115200, 8 bits, no parity and 1 stop bit.
3. Connect a power supply of +5V capable of providing at least 500mA (supplied: Center +ve).
4. Check Boot Flash Write Enable setting : No jumper fitted to J5 pins 1-2
5. Check Main Flash Write Enable setting: Jumper is fitted to J5 pins 3-4
6. Check Monitor Enable setting: No jumper fitted to J5 pins 5-6
7. Check Boot Mode setting: Jumper is fitted to J5 pins 7-8
8. Switch Power on.

# 6. CODE DEVELOPMENT

Incorporated into the mot file that is programmed into the Boot Flash device is the option to run the Embedded Test Suite software (ETS). This software is available to the user, via a hyper-terminal link and contains a number of functions including the choice of testing the major functions of the EDOSK and the option of downloading user software to both the AMD and INTEL Flash devices.

## 6.1. FLASH PROGRAMMING

EDOSK hardware allows both Boot and Main Flash memory to be programmed in system when the appropriate write enable jumpers are fitted.

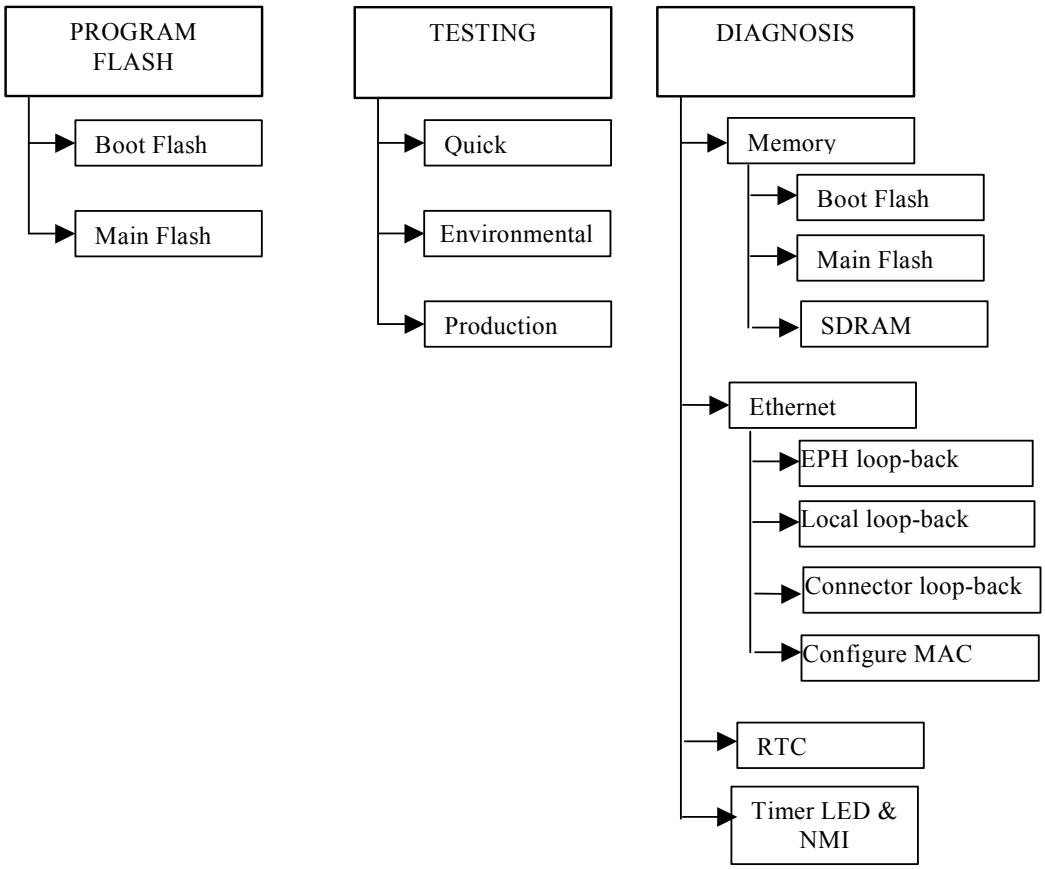
When the EDOSK is first powered up in Boot mode and a serial connection has been made to a hyper terminal the user will be given the option to re-program Flash devices.

The user may specify any valid S-Record file to be programmed.

## 6.2. TEST MENU

The tests incorporated in the Boot Flash allow for a majority of the EDOSK to be verified – for production and for prototype debugging.

Three main menu options are given to Program Flash, Testing and Diagnosis. These lead to further menu options as shown below:




## 6.3. HDI-MONITOR

The H8/2674R has no dedicated debug port and at present SW has not been developed to enable a HDI monitor for the EDOSK2674.

However, a MON_EN (monitor enable) jumper has been provided for this future feature. This jumper drives MCU port pin 30 Low when fitted and High when not fitted. HDI-Monitor code may be integrated with the user code and read the monitor enable jumper setting to enable or disable the feature.

# 7. SOFTWARE

The following map and register settings are for the H8/2674R fitted to the EDOSK2674 as standard i.e. with a system clock frequency of 33MHz.

Registers are subject to change depending on the software requirements.

## 7.1. EDOSK2674 MEMORY MAP

The addressable memory address space is split into eight areas, each capable of addressing 2Mbytes. Each area has a dedicated chip select signal (CS0n – CS7n). – Note that these signals are only enabled when PFCR0 register bits are set.

Mode of the system determines which memory resides in areas 0 and 1.

The following table shows the EDOSK2674 memory map and bus width.

| FROM | TO | External Area | Description | Size | Bus Width |
|---|---|---|---|---|---|
| **MODE :** | | **BOOT** | | | |
| H'000000 | H'1FFFFF | CS0 | Boot FLASH (***note 1***) | 512KB x4 | 8 |
| H'200000 | H'3FFFFF | CS1 (Port pin Low) | Main FLASH (page 0) | 2MB | 16 |
| H'200000 | H'3FFFFF | CS1 (Port pin High) | Main FLASH (page 1) | 2MB | |
| **MODE :** | | **NORMAL** | | | |
| H'000000 | H'1FFFFF | CS0 | Main FLASH (page 0) | 2MB | 16 |
| H'200000 | H'3FFFFF | CS1 | Main FLASH (page 1) | 2MB | |
| **MODE :** | | **NORMAL & BOOT** | | | |
| H'400000 | H'BFFFFF | CS2,CS3,CS4,CS5 | SDRAM | 8MB | 16 |
| H'C00000 | H'DFFFFF | CS6 | Expansion board | 2MB | 8/16 |
| H'E00000 | H'EFFFFF | CS7 | Boot FLASH (***note 1***) | 512KB x2 | 8 |
| H'F00000 | H'F7FFFF | CS7 | TBD | 0.5MB | |
| H'F80000 | H'FBFFFF | CS7 | LAN CHIP (***note 2***) | 256KB | |
| H'FC0000 | H'FF3FFF | CS7 | TBD | 208KB | |
| H'FF4000 | H'FFBFFF | CS7 | On Chip RAM (***note 3***) | 32KB | |
| H'FFC000 | H'FFFBFF | CS7 | External address space | 15 KB | |
| H'FFFC00 | H'FFFEFF | CS7 | Internal I/O registers | 768B | |
| H'FFFF00 | H'FFFF1F | CS7 | External address space | 32B | |
| H'FFFF20 | H'FFFFFF | CS7 | Internal I/O registers | 224B | |

**TABLE 7-1: MEMORY MAP**

Note 1: The same 512K of Boot FLASH is mapped 4 times over the 2MB area of CS0 (in Boot mode only) and 2 times over the 1MB area.

Note 2: LAN only occupies 16 bytes (0x0 to 0xF), but is repeated throughout the 256KB mapped area.

Note 3: Only if internal RAM is enabled.

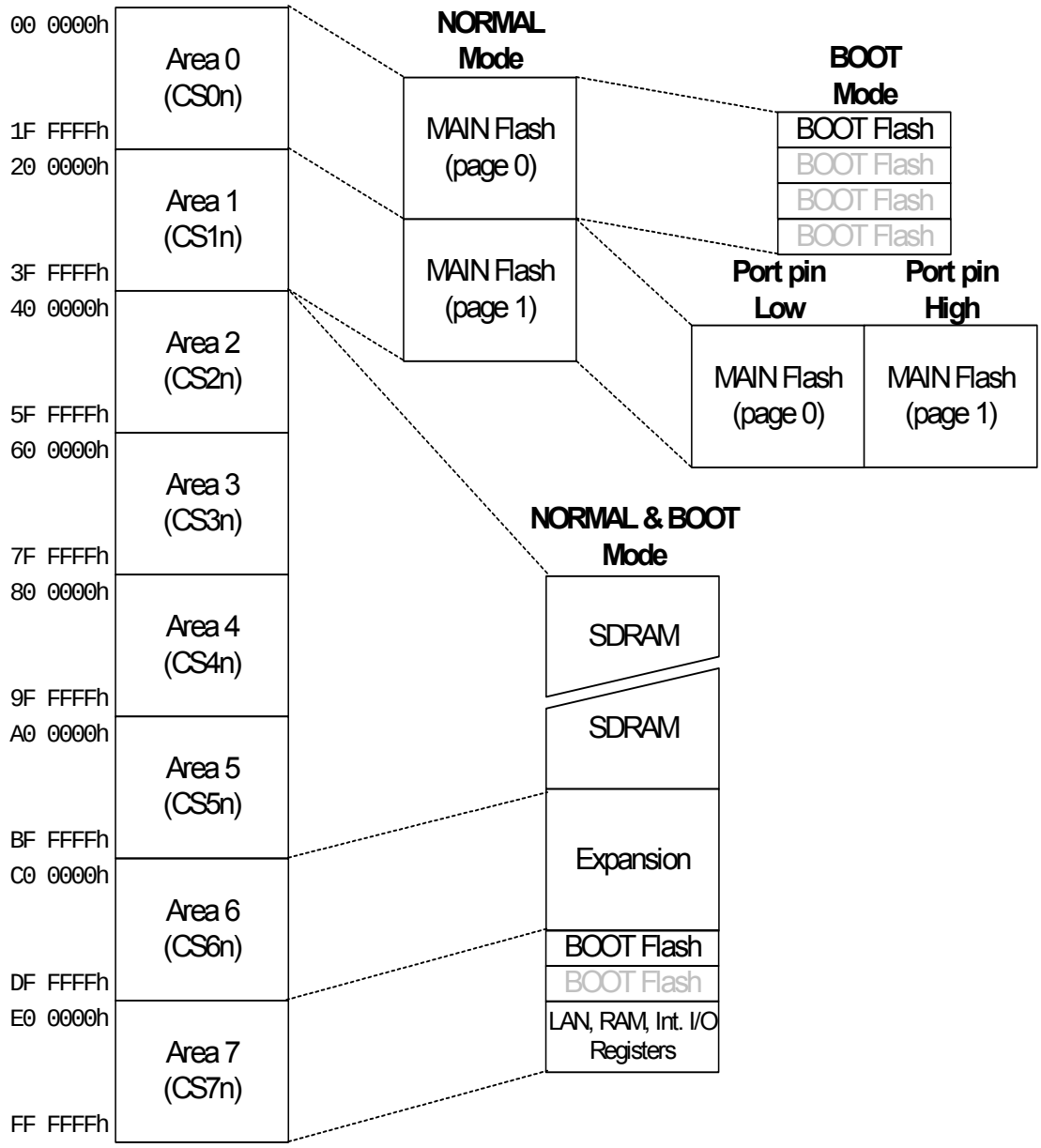



**FIGURE 7-1: MEMORY MAP**

In Normal mode the Main Flash pages 0 and 1 are mapped to areas 0 and 1 respectively. Port pin 33 is not used. The Boot Flash may only be accessed in area 7.

In Boot mode the Main Flash is mapped to area 1 only and driving Port 33 Low or High selects page 0 or 1. The Boot Flash is duplicated in areas 0 and 7.

## 7.2. H8/2674R REGISTER CONFIGURATION

### 7.2.1. BUS CONTROLLER (BSC)

**Bus Width Control Register:**

**ABWCR (H'FFFEC0) = H'81 (BOOT) or H'80 (NORMAL)**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | ABW7 | ABW6 | ABW5 | ABW4 | ABW3 | ABW2 | ABW1 | ABW0 |
| Initial Value | 1 or 0 | 1/0 | 1/0 | 1/0 | 1/0 | 0 | 0 | 1 |

Note: In BOOT mode (MCU mode 2), ABWCR is initialized to 1. In NORMAL mode (MCU mode 1), ABWCR is initialized to 0.

In BOOT mode area 7 and 0 are mapped as 8-bit areas.

In NORMAL mode only area 7 is mapped as 8-bit area.

The SDRAM (ABW2) is always mapped as 16-bit area.

**Access State Control Registers:**

**ASTCR (H'FFFEC1) = H'FF**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | AST7 | AST6 | AST5 | AST4 | AST3 | AST2 | AST1 | AST0 |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

All areas are designated as 3-state access space.

**Wait Control Registers:**

**WTCRAH (H'FFFEC2) = H'27**

| Bit No | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | W72 | W71 | W70 | Reserved | W62 | W61 | W60 |
| Initial Value | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |

Area 7 has 2 program wait states inserted.

Area 6 has 7 program wait states inserted.

**WTCRAL (H'FFFEC3) = H'77**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | W52 | W51 | W50 | Reserved | W42 | W41 | W40 |
| Initial Value | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

Area 5 has 7 program wait states inserted.

Area 4 has 7 program wait states inserted.

**WTCRBH (H'FFFEC4) = H'71**

| Bit No | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | W32 | W31 | W30 | Reserved | W22 | W21 | W20 |
| Initial Value | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

Area 3 has 7 program wait states inserted.

SDRAM has a CAS Latency of 2.

**WTCRBL (H'FFFEC5) = H'23 (BOOT) or H'22 (NORMAL)**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | W12 | W11 | W10 | Reserved | W12 | W11 | W10 |
| Initial Value | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 or 0 |

Area 1 has 2 program wait states inserted.

In BOOT mode, area 0 has 3 program wait states inserted.

In NORMAL mode area 0 has 2 program wait states inserted.

**Read Strobe Timing Control Register:**

**RDNCR (H'FFFEC6) = H'00**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RDN7 | RDN | RDN | RDN | RDN | RDN | RDN | RDN |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

In all areas the /RD signal is negated at the end of the read cycle.

**CS assertion Period Control Registers:**

**CSACRH (H'FFFEC8) = H'80**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CSXH7 | CSXH6 | CSXH5 | CSXH4 | CSXH3 | CSXH2 | CSXH1 | CSXH0 |
| Initial Value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

In area 7 basic bus interface access, the /CSn and address assertion period ($T_h$) is extended.

**CSACRL (H'FFFEC9) = H'80**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CSXT7 | CSXT6 | CSXT5 | CSXT4 | CSXT3 | CSXT2 | CSXT1 | CSXT0 |
| Initial Value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

In area 7 basic bus interface access, the /CSn and address assertion period ($T_t$) is extended.

**Burst ROM Interface Control Register:**

**BROMCRH (H'FFFECA) = H'D3 (BOOT) or H'A3 (NORMAL)**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BSRMn | BSTSn2 | BSTSn1 | BSTSn0 | Reserved | Reserved | BSWDn1 | BSWDn0 |
| Initial Value | 1 | 1 or 0 | 0 or 1 | 1 or 0 | 0 | 0 | 0 | 0 |

Area 0 burst ROM enabled with maximum of 4 words.

In BOOT mode 6-cycle burst states are used.

In NORMAL mode 3-cycle burst states are used.

**BROMCRL (H'FFFECB) = H'A3**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BSRMn | BSTSn2 | BSTSn1 | BSTSn0 | Reserved | Reserved | BSWDn1 | BSWDn0 |
| Initial Value | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

Area 1 burst ROM enabled with maximum of 4 words.

3-cycle burst states are used.

**Bus Control Register:**

**BCR (H'FFFECC) = H'0100**

| Bit No | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BRLE | BREQOE | Reserved | IDLC | ICIS1 | ICIS0 | WDBE | WAITE |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | Reserved | Reserved | Reserved | Reserved | ICIS2 | Reserved | Reserved |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

External bus release and bus request disabled, no idle cycles inserted, WAIT pin enabled

**DRAM control register:**

**DRAMCR (H'FFFED0) = H'84B4**

| Bit No | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | OEE | RAST | Reserved | CAST | Reserved | RMTS2 | RMTS1 | RMTS0 |
| Initial Value | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BE | RCDM | DDS | EDDS | Reserved | MXC2 | MXC1 | MXC0 |
| Initial Value | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

OE/CKE signal output enabled, RAS is asserted from ∅ falling edge in $T_1$ cycle, 2-state column address cycle, Continuous synchronous DRAM space

Access in fast page mode, 8-Bit shift, Row address bits A23 to A12 used for comparison, The precharge-sel is A15 to A12 of the column address.

**SDRAM Notes:**

Prior to using the SDRAM the mode must be set in the SMR (SDRAM Mode Register).

The SMR should be set to the value B'0000 0010 0000 – CAS latency 2, Burst 1. This is achieved by a write cycle to the SDRAM at an address equal to the required SMR value when in configuration mode.

The address to set the SMR should be H'400040 – SDRAM starts at area H'400000 and the SMR value must be shifted to compensate for word access.

Example:

1. Configure all other SDRAM Registers.
2. DRAMCR = 0x85B4; //SMR configuration mode
3. SDRAM_CONTROL = 0; // where SDRAM_CONTROL is H'400040
4. DRAMCR = 0x84B4; //Return to SDRAM operating mode

**DRAM Access Control Register:**

**DRACCR (H'FFFED2) = H'0000**

| Bit No | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | DRMI | Reserved | TPC1 | TPC0 | SDWCD | Reserved | RCD1 | RCD0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | Reserved | Reserved | Reserved | CKSPE | Reserved | RDXC1 | RDXC0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Idle cycle not inserted, 1-State Pre-charge, CAS latency enabled, No wait between RAS and CAS cycles.

No clock suspend, 1-State read data extension cycle.

**Refresh Control Register:**

**REFCR (H'FFFED4) = H'0188**

| Bit No | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CMF | CMIE | RCW1 | RCW0 | Reserved | RTCK2 | RTCK1 | RTCK0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RFSHE | CBRM | RLW1 | RLW0 | SLFRF | TPCS2 | TPCS1 | TPCS0 |
| Initial Value | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

No wait states between CAS and RAS, REF count on ∅/2

Enable refresh control, No waits for CAS-before-RAS refresh cycle, Self refresh enabled, zero states in the precharge cycle immediately after self refreshing.

**Refresh Timer Counter:**

**RTCNT (H'FFFED6 ) = H'FF**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RTCNT7 | RTCNT6 | RTCNT5 | RTCNT4 | RTCNT3 | RTCNT2 | RTCNT1 | RTCNT0 |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Refresh Time Constant Register:**

**RTCOR (H'FFFED7) = H'FF**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RTCOR7 | RTCOR6 | RTCOR5 | RTCOR4 | RTCOR3 | RTCOR2 | RTCOR1 | RTCOR0 |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Compare refresh count with 0xFF

### 7.2.2. INTERRUPT CONTROLLER

The EDOSK2674 only uses the following interrupts:

- IRQ5n – Main Flash
- IRQ0n – LAN Controller
- IRQ1n-IRQ5n – Expansion connector
- NMI – Switch

**Interrupt Control Register:**

**INTCR (H'FFFF31) = H'08**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | Reserved | INTM1 | INTM0 | NMIEG | Reserved | Reserved | Reserved |
| Initial Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

NMI is rising edge triggered. Interrupt Control mode 0

**IRQ Pin Select Register:**

**ITSR (H'FFFE16) = H'FF3F**

| Bit No | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | ITS15 | ITS14 | ITS13 | ITS12 | ITS11 | ITS10 | ITS9 | ITS8 |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | ITS7 | ITS6 | ITS5 | ITS4 | ITS3 | ITS2 | ITS1 | ITS0 |
| Initial Value | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

IRQ15-IRQ8 – Port 2

IRQ7,6 – Port 57, 56

IRQ5-IRQ0 – Port 8

### 7.2.3. SERIAL COMMUNICATION INTERFACE 2

**Serial Extension Mode Register:**

**SEMR (H'FFFDA8) = H'00**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | Reserved | Reserved | Reserved | ABCS | ACS2 | ACS1 | ACS0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Basic Clock is External; this register is not used.

**Serial Mode Register_2:**

**SMR_2 (H'FFFF88) = H'00**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | C/A | CHR | PE | O/E | STOP | MP | CKS1 | CKS0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Asynchronous, 8-bit, No Parity, 1-Stop bit, Clock source ∅

**Bit Rate Register_2:**

**BRR_2 (H'FFFF89) = H'FF**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BRR7 | BRR6 | BRR5 | BRR4 | BRR3 | BRR2 | BRR1 | BRR0 |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

This register is not used.

**Serial Control Register_2:**

**SCR_2 (H'FFFF8A) = H'32**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | TIE | RIE | TE | RE | MPIE | TEIE | CKE1 | CKE0 |
| Initial Value | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

Interrupt settings depend on SW, External Clock input 16 times bit rate.

**Smart Card Mode Register_2:**

**SCMR_2 (H'FFFF8E) = H'F2**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | Reserved | Reserved | Reserved | SDIR | SINV | Reserved | SMIF |
| Initial Value | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |

Smart Cart Interface mode not used.

### 7.2.4. WATCHDOG TIMER

**Timer Control/Status Register:**

**TCSR (H'FFFFBC) = H'18**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | OVF | WT/IT | TME | Reserved | Reserved | CKS2 | CKS1 | CKS0 |
| Initial Value | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

**Timer Counter:**

**TCNT (H'FFFFBC-write / H'FFFFBD-read) = H'00**

TCNT is an 8-bit readable/writable up-counter. TCNT is initialized to H'00 when the TME bit in TCSR is cleared to 0.

**Reset Control/Status Register:**

**RSTCSR (H'FFFFBE) = H'1F**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | WOVF | RSTE | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Initial Value | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

To prevent accidental overwriting, access of WDT registers is different from other registers.

The WDT may be used to drive the 'TIMER' LED when the counter overflows. This, however, is a very short period and in order to see the LED with the naked eye the WDT must be forced to overflow repeatedly.

Example to keep LED on:

```
TCSR = 0xA500; // clear lower byte.
TCSR = 0xA578; // setup & Enable the watchdog timer.
while( 1)
{
        if( RSTCSR & 0x0080 ) // detect overflow and reset WDT.
        {       RSTCSR = 0xA500; // clear watchdog overflow bit.
                TCSR = 0xA578;   // clear overflow bit and enable WDT.
        }
}
```

### 7.2.5. IO PORT

**Port Function Control Register 0:**

**PFCR0 (H'FFFE32) = H'FF**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CS7E | CS6E | CS5E | CS4E | CS3E | CS2E | CS1E | CS0E |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Enable all CS signals

**Port Function Control Register 1:**

**PFCR1 (H'FFFE33) = H'FF**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | A23E | A22E | A21E | A20E | A19E | A18E | A17E | A16E |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Enable all Address lines (A21 and A23 used for SDRAM bank select)

**Port Function Control Register 2:**

**PFCR2 (H'FFFE34) = H'0D**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | Reserved | Reserved | Reserved | ASOE | LWROE | OES | DMACS |
| Initial Value | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

PF6 is designated as /AS output pin.

PF3 is designated as /LWR output pin.

P35 is designated as SDRAM CKE output pin.

PF75 to PF70 are designated as DMAC control pins

| MCU Port 3 | Signal Name | Function |
|---|---|---|
| 30 | MON_ENn | Monitor Enable. Active Low. Enables monitor functions embedded in software. |
| 31 | I2C_SCL | I2C bus serial clock for RTC |
| 32 | I2C_SDA | I2C bus serial data signal to/from RTC |
| 33 | MFLASH_PAGE | Main Flash page select. Used in Boot mode only. Low selects page 0, High selects page 1 |
| 34 | SDRAM_CSn | SDRAM chip select. Active Low. Enables the SDRAM device. |
| 35 | SDRAM_CKE | SDRAM clock enable. Active Low. Enables the SDRAM clock input. |

**Port 3 Data Direction Register:**

**P3DDR (H'FFFE22) = H'3A**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | Reserved | P35DDR | P34DDR | P33DDR | P32DDR | P31DDR | P30DDR |
| Initial Value | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |

The individual bits of P3DDR specify input or output for the pins of port 3 – '0' input, '1' output.

**Port 3 Data Register:**

**P3DR (H'FFFF62) = H'00**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | Reserved | P35DR | P34DR | P33DR | P32DR | P31DR | P30DR |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

P3DR stores output data for the port 3 pins.

Enable SDRAM CS.

**Port 3 Register:**

**PORT3 (H'FFFF52)**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | Reserved | P35 | P34 | P33 | P32 | P31 | P30 |
| Initial Value | 0 | 0 | X | X | X | X | X | X |

Read only, value determined by the states of pins P35 to P30.

**Port 3 Open Drain Control Register:**

**P3ODR (H'FFFE3C) = H'06**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | Reserved | P35ODR | P34ODR | P33ODR | P32ODR | P31ODR | P30ODR |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

I2C signals are NMOS open-drain

**Port A Data Direction Register:**

**PADDR (H'FFFE29) = H'FF**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | PADDR | PADDR | PADDR | PADDR | PADDR | PADDR | PADDR | PADDR |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The individual bits of PADDR specify input or output for the pins of port A – '0' input, '1' output.

**Port F Data Direction Register:**

**PFDDR (H'FFFE2E) = H'FE**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | PFDDR | PFDDR | PFDDR | PFDDR | PFDDR | PFDDR | PFDDR | PFDDR |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

The individual bits of PFDDR specify input or output for the pins of port F – '0' input, '1' output.

Set all as outputs except PF0 (WAITn)

**Port G Data Direction Register:**

**PGDDR (H'FFFE2F) = H'0F**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | PGDDR | PGDDR | PGDDR | PGDDR | PGDDR | PGDDR | PGDDR |
| Initial Value | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

The individual bits of PGDDR specify input or output for the pins of port G – '0' input, '1' output.

**Port H Data Direction Register:**

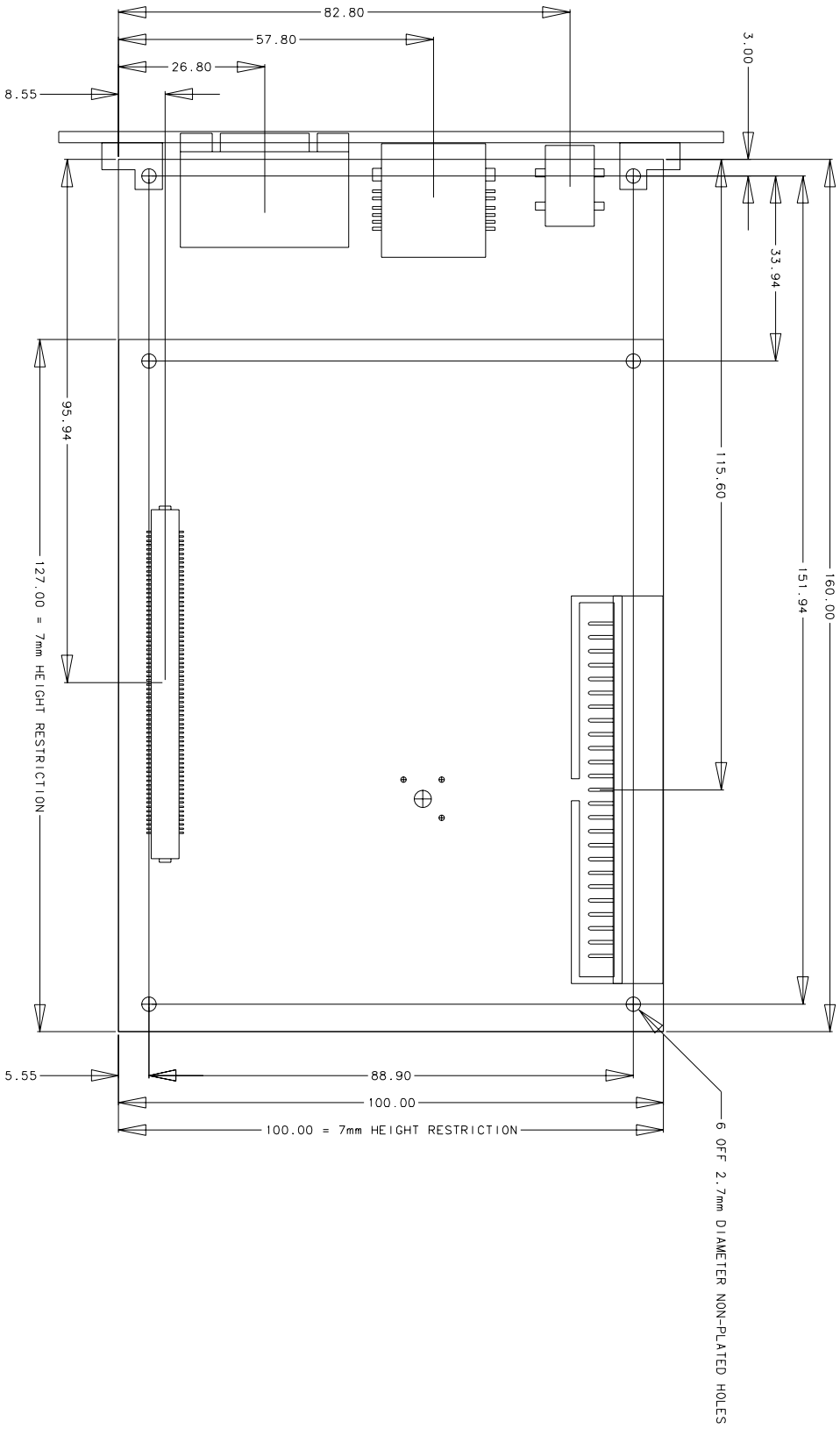
**PHDDR (H'FFFF74) = H'0F**

| Bit No | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Reserved | Reserved | Reserved | Reserved | PHDDR | PHDDR | PHDDR | PHDDR |
| Initial Value | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

The individual bits of PHDDR specify input or output for the pins of port H – '0' input, '1' output.

# 8. MECHANICAL DRAWING

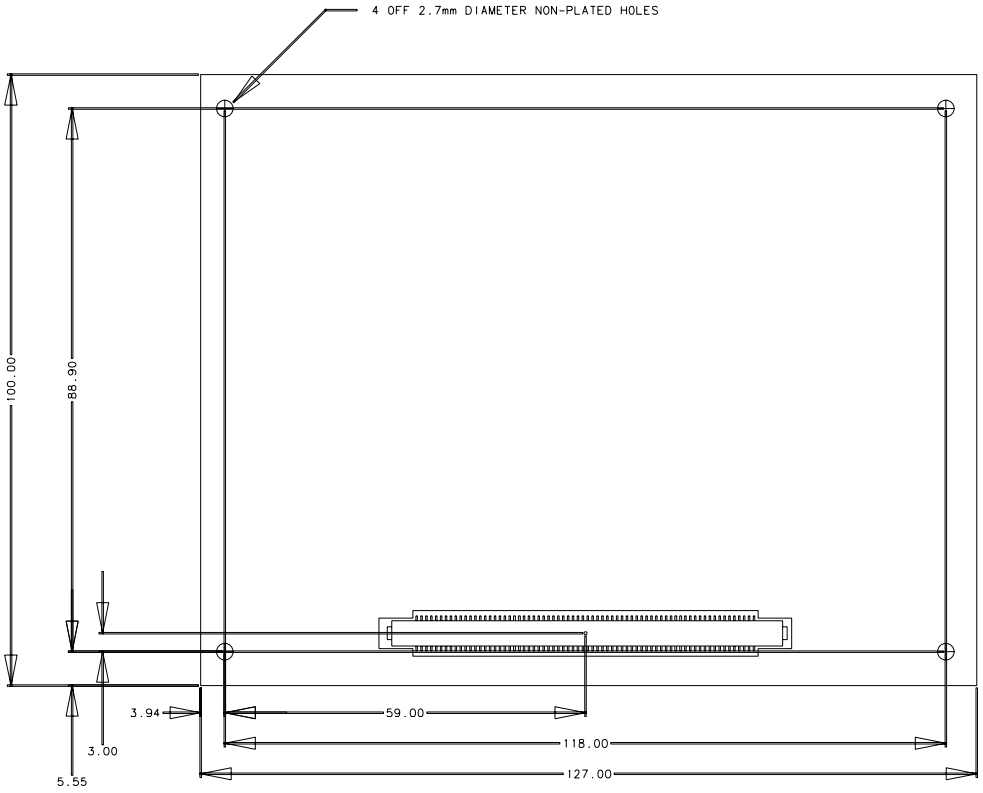
The mechanical drawing has been included here for the user to develop add-on boards and face plates.



# 9. DESIGNING AN EXPANSION CARD

## 9.1. MECHANICAL

The Expansion Card should be designed using the following dimensions (viewed from the top looking through the board at the connector):




The JAE connector KX15-140K2D (shown) is fitted to the under-side of the Expansion Card to mate with KX14-140K5D of the main board (in this case the EDOSK2674) with board to board space of 7mm. Components fitted to the under-side of the Expansion Card must have a maximum height of 2mm.

Both connectors are surface mounted and therefore another KX14-140K5D may be fitted to the top-side of the Expansion Card to allow stacking.

The 4 off 2.7mm holes in the corners are for stand-off fixings.

## 9.2. FUNCTIONAL

Consideration must be given to the following connecting signals.

**Reset Signal**

The Expansion connector has a dedicated active low Reset signal (RESn).

When low all devices fitted to the plug-in board should be reset.

*EDOSK2674 Limitations-*

RESn signal may be used.

**System Clock**

The Expansion connector has a dedicated System Clock signal (CKIO).

This clock may be used for bus cycle timing but may vary in frequency depending upon the main board used.

It is recommended that this clock is correctly terminated and/or buffered if being used.

*EDOSK2674 Limitations-*

CKIO signal may be used but is not buffered.

**Chip Select**

There are 7 active low chip select signals dedicated to the Expansion connector (CS0n to CS6n).

Theses are used to select 7 areas of external memory.

To avoid contention the plug-in hardware should have the facility to select which of these is to be used.

*EDOSK2674 Limitations-*

BOOT mode (H8 mode 2: 8-bit):

CS0n may be used if the AMD Boot Flash is removed.

CS1n may be used if R37 0Ω resistor is fitted.

NORMAL mode (H8 mode 1: 16-bit):

CS0n and CS1n may be used if R37 0Ω resistor is fitted.

Note that in this mode areas 0 and 1 can not be isolated.

CS2n to CS5n are not connected.

CS6n may be used.

**Address Bus**

There are 26 Address lines dedicated to the Expansion connector (A0 to A25).

This allows for address mapping of 2^26 Bytes = 64MB.

*EDOSK2674 Limitations-*

A0 to A23 may be used (16MB maximum).

A24 and A25 are not connected

**Data Bus**

There are 32 Data lines dedicated to the Expansion connector (D0 to D31).

This allows data to be accessed as Byte (8-bit), Word (16-bit) or long (32-bit).

*EDOSK2674 Limitations-*

D0 to D15 may be used (Byte or Word access).

D16 to D31 are not connected.

Note: For an 8-bit mapped area D8 to D15 must be used.

**Read-Write Strobe**

The Expansion connector has a dedicated Read-Write signal (RWn).

High indicates a read cycle and Low indicates a write cycle.

*EDOSK2674 Limitations-*

RWn signal is not connected.

**Read Strobe**

The Expansion connector has a dedicated active low Read strobe (RDn).

*EDOSK2674 Limitations-*

RDn signal may be used.

**Write Strobe**

There are 4 active low Write Enable signals dedicated to the Expansion connector (WE0n to WE3n).

A 32-bit data bus may be separated into 4 bytes, the Write Enable signals are used to determine which of those bytes are to be written.

*EDOSK2674 Limitations-*

WE0n may be used to enable write data on D0 to D7.

WE1n may be used to enable write data on D8 to D15.

WE2n and WE3n are not connected.

Note: For an 8-bit mapped area WE1n must be used.

**Bus Strobe**

The Expansion connector has a dedicated active low Bus strobe (BSn).

When low, this signifies the beginning of a bus cycle or it may be used for latching the address while in MPX mode.

*EDOSK2674 Limitations-*

BSn signal may be used.

Note: H8S2674R does not support MPX mode.

**Wait**

There are 4 active low WAIT signals dedicated to the Expansion connector (WAIT0n to WAIT3n).

These are used to hold off the bus cycle until the device being accessed is ready.

To avoid contention the plug-in hardware should have the facility to select which of these is to be used.

*EDOSK2674 Limitations-*

WAIT0n may be used.

WAIT1n to WAIT3n is not connected.

**Interrupts**

There are 8 Interrupt Request signals dedicated to the Expansion connector (IRQ1n to IRQ8n).

These are used to interrupt the main board processor. Depending upon the MCU IRQ may be level and/or edge triggered.

To avoid contention the plug-in hardware should have the facility to select which of these is to be used.

*EDOSK2674 Limitations-*

IRQ1n to IRQ4n may be used.

IRQ5n may be used, but is also used by the Main Flash.

IRQ6n to IRQ8n are not connected.

**Direct Memory Access**

There are 2 DMA request and 2 DMA acknowledge, all active low, signals dedicated to the Expansion connector (DREQ0n, DREQ1n, DACK0n and DACK1n).

These are used by the plug-in hardware to request and acknowledge a faster memory access.

To avoid contention the plug-in hardware should have the facility to select which of these is to be used.

*EDOSK2674 Limitations-*

All DMA signals may be used.

# 10. ADDITIONAL INFORMATION

For details on how to use Hitachi Embedded Workshop (HEW) refer to the HEW manual available on the CD or from the web site.

For information about the H8 series microcomputers refer to the *H8 Series Hardware Manual*

For information about the assembly language, refer to the *H8 Series Programming Manual*

Further information available for this product can be found on the HMSE web site at:

http://www.hmse.com/products/edosk

General information on Hitachi microcomputers can be found at the following URL.

Global: http://www.hitachisemiconductor.com/